IN THE SPECIFICATION

Replace the paragraph beginning on page 4, line 21, and continuing to page 5, line 2, with:

Memory system 10 includes a state machine and general logic block 14 for controlling operation of memory system 10. State machine 14 is coupled to a program pump 22 and to an erase pump 24 for respectively implementing program and erase operations relative to a memory block 16. For example, pumps 22 and 24 each receive a voltage control channel (VCC) signal to supply a boosted voltage. Pumps 22 and 24 are further coupled to regulator circuits 26 and 28, respectively, and transfer high voltage signals to their associated regulator circuits. Voltage regulator circuits 26 and 28 receive a reference voltage signal from a reference voltage generator 30, which is activated in response to a State Machine On (SMON) signal. Typically, the reference voltage signal from reference voltage generator 30 ramps up to a desired voltage level upon beginning a program/erase operation or a program/erase verify operation. Regulator circuits 26 and 28 are coupled to memory block 16 and, in particular, to the decoders comprising memory block 16. Regulator circuits 26 and 28 produce controlled voltage signals based on the reference voltage, which controlled voltage signals are selectively applied to the sources of the floating gate memory cells.

Replace the paragraph on page 10, lines 11-23, with:

Latch 270 comprises a pair of inverters 274 and 276 coupled such that the output terminal of inverter 274 is connected to the input terminal of inverter 276 to form the input terminal of latch 270 and the output terminal of inverter 276 is connected to the input terminal of inverter 274 to form the output terminal of latch 270. The output terminal of latch 270 is coupled to an input terminal of a complementary passgate 280 through an inverter 278. Passgate 280 has a control terminal coupled for receiving a control signal MAXCBIT from terminal 254 and a complementary control terminal coupled through an inverter 252 for receiving control signal MAXCBIT. The output

terminal of passgate 280 is coupled to output terminal 256 for transmitting the data signal PODINn. It should be noted that the output terminal of passgate 280 is also connected to the output terminal of passgate 250. When I/O data signal PODINn is transmitted from passgate 250 it is a refresh signal for the normal data bits, whereas when I/O data signal PODINn is transmitted from passgate 280 it is a refresh signal for the complementary data bits.

Replace the paragraph beginning on page 11, line 33, and continuing to page 12, line 29, with:

In Byte mode programming, before programming begins a refresh read step is performed to determine which bits need to be refreshed. In an embodiment in which the high byte of the stored word is refreshed before the low byte of the stored word is refreshed, a read refresh step is performed to refresh the high byte of the stored word. Thus, control signal DLBH is maintained at a logic low voltage level so that passgates 210 of the corresponding I/O buffer circuits 118-132, i.e., the high byte, are not opened. For bits of the high byte of the stored word that have been programmed and are to be refreshed, status control signal DSIBWn is raised to a logic high voltage level. A logic low voltage level is also referred to as a logic low level and a logic high voltage level is also referred to as a logic high level. By way of example, a logic low level ranges from approximately –0.5 volts to approximately 1.8 volts and a logic high level ranges from approximately 2.5 volts to approximately 4 volts. In addition, enable signals RFNBIT and RFRESHENH are pulsed to a logic high level and enable signal RFRESHENL is maintained at a logic low level. More particularly, enable signal RFNBIT is pulsed to a logic high level during the first half of a first clock cycle, thereby placing memory system 10 in the READ refresh mode to refresh the normal bits of the high byte. Likewise, during the first half of the first clock cycle RFRESHENH is pulsed to a logic high level to allow the bits located in the high byte of the stored word having a logic low or zero value to set corresponding latches 204 in I/O buffer circuits 118-132. For example, if bit n has been programmed, status control signal DSIBWn is set to a logic high level, refresh enable signal RFRESHENH is pulsed to a logic high level and a logic low or zero is

stored at node G2. Control signal ~~DLBL~~ DLBH is pulsed high to allow input data DINDn to be ORed with the logic low value appearing at node G2 to generate an updated latch value. This updated latch value is also referred to as a refresh value. Thus, a logic operation, i.e., an Oring operation, is performed on a value from the first memory location, i.e., the value appearing at node G2 and data value DINDn. The refresh value appearing at node G2 is inverted by latch 234 and appears at node H2. The inverted signal appearing at node H2 is inverted by inverter 248 and transmitted to output terminal 256 via passgate 250, which is activated by setting signal control signal MAXCBIT to a logic low level and control signal MAXCBITB to a logic high level. Thus, the logic low level refresh signal stored at node G2 is transmitted to output terminal 256 where it is referred to as input/output (I/O) signal PODINn. I/O signal PODINn serves as an input signal at input terminal 312 of write latching portion 300 (shown in FIG. 5).

Replace the paragraph beginning on page 12, line 30, and continuing to page 13, line 2, with:

During the second half of the first clock cycle, enable signal WLOAD is pulsed to a logic high level and enable signal RFNBIT is set to a logic low level, thereby latching the refresh signal in write latching portion 300. In other words, passgate 310 is opened and the refresh signal is transferred to node G, latched by latch 334, and appears at output terminal 350 as output signal DOUTDn. Output signal DOUTDn updates or refreshes the corresponding bit of the word. Thus, the updated latch value is written from data I/O circuit 100 to a memory location in memory array 16 in response to enable or control signal DSIBWn which is indicative of the data value and in response to enable or control signal RFNBIT which is indicative of the status of the read operation. It should be noted that output signal DOUTDn is the signal of the complementary bit.

Replace the paragraph on page 13, lines 5-24, with:

During the second half of the second or subsequent clock cycle, the complementary bits for the entire or whole word are refreshed. Status control signal

DSIBWn remains at a logic high level and, during the second half of the second clock cycle, enable signal RFCBIT is pulsed to a logic high level. Thus, a logic low level is placed on node G1, which logic low level sets corresponding latches 210 in I/O buffer circuits 118-132. For example, if bit n has been programmed, status control signal DSIBWn is set to a logic high level and a logic low or zero is stored at node G1. The logic low level or complementary refresh value appearing at node G1 is inverted by latch 270 and appears at node H1. The inverted signal appearing at node H1 is inverted by inverter 278 and transmitted to output terminal 256 via passgate 278, which was activated by setting control signal MAXCBIT to a logic high level and control signal MAXCBITB to a logic low level. Thus, the logic low level refresh signal stored at node G1 is transmitted to output terminal 256 where it becomes input/output (I/O) signal PODINn. I/O signal PODINn serves as an input signal at input terminal 312 (shown in FIG. 5). Also during the second half of the second clock cycle, enable signal WLOAD is set to a logic high level, thereby latching the refresh signal in write latching portion 300. In other words, passgate 310 is opened and the refresh signal is transferred to node G, latched by latch 334, and appears at output terminal 350 as output signal DOUTDn. Output signal DOUTDn updates or refreshes the corresponding bit of the word. Thus, the updated latch value is written from data I/O circuit 100 to a memory location in memory array 16 in response to enable or control signal DSIBWn which is indicative of the data value and in response to enable or control signal RFCBIT which is indicative of the status of the read operation. It should be noted that output signal DOUTDn is the output signal of the complementary bit.

Replace the paragraph beginning on page 13, line 25, and continuing to page 14, line 24, with:

During a third clock cycle, the low byte of the word is refreshed. In the first half of the third clock cycle, a control signal DLBL is maintained at a logic low level so that passgates 210 of the corresponding I/O buffer circuits 102-116, i.e., the low byte, are not opened. For bits of the low byte of the stored word that have been programmed and are to be refreshed, status control signal DSIBWn is raised to a logic high level. In addition, enable signals RFNBIT and RFRESHENL are pulsed to a logic high level. More

particularly, RFNBIT is pulsed to a logic high level during the first half of the third clock cycle, thereby placing memory system 10 in the READ refresh mode to refresh the normal bits of the low byte. Likewise, during the first half of the third clock cycle RFRESHENL is pulsed to a logic high level to allow the bits located in the high byte of the stored word having a logic low or zero value to set corresponding latches 204 in I/O buffer circuits 102-116. For example, if bit n has been programmed, status control signal DSIBWn is set to a logic high level, refresh enable signal RFRESHENL is pulsed to a logic high level and a logic low or zero is stored at node G2. Control signal DLBH is pulsed high to allow input data DINDn to be ORed with the logic low value appearing at node G2 to generate an updated latch value. This updated latch value is also referred to as a refresh value. Thus, a logic operation, i.e., an Oring operation, is performed on a value from the first memory location, i.e., the value appearing at node G2 and data value DINDn. The refresh value appearing at node G2 is inverted by latch 234 and appears at node H2. The logic low level appearing at node G2 is inverted by latch 234 and appears at node H2. The inverted signal appearing at node H2 is inverted by inverter 248 and transmitted to output terminal 256 via passgate 250, which was activated by setting control signal MAXCBIT to a logic low level and control signal MAXCBITB to a logic high level. Thus, the logic low level refresh signal stored at node G2 is transmitted to output terminal 256 where it is referred to as input/output (I/O) signal PODINn. I/O signal PODINn serves as an input signal at input terminal 312 (shown in FIG. 5). During the second half of the third ~~first~~ clock cycle, enable signal WLOAD is set to a logic high level and enable signal RFNBIT is set to a logic low level, thereby latching the refresh signal in write latching portion 300. In other words, passgate 310 is opened and the refresh signal is transferred to node G, latched by latch 334, and appears at output terminal 350 as output signal DOUTDn. Output signal DOUTDn updates or refreshes the corresponding bit of the word. Thus, the updated latch value is written from data I/O circuit 100 to a memory location in memory array 16 in response to enable or control signal DSIBWn which is indicative of the data value and in response to enable or control signal RFNBIT which is indicative of the status of the read operation. It should be noted that output signal DOUTDn is the signal for the complementary bit. It should be understood that the clock cycles have been numbered as first, second, and third merely

for the sake of clarity and the numbering is not a limitation of the present invention. In other words, the clock cycle numbering illustrates the relative timing relationship of the clock cycles and not the actual clock cycle number.